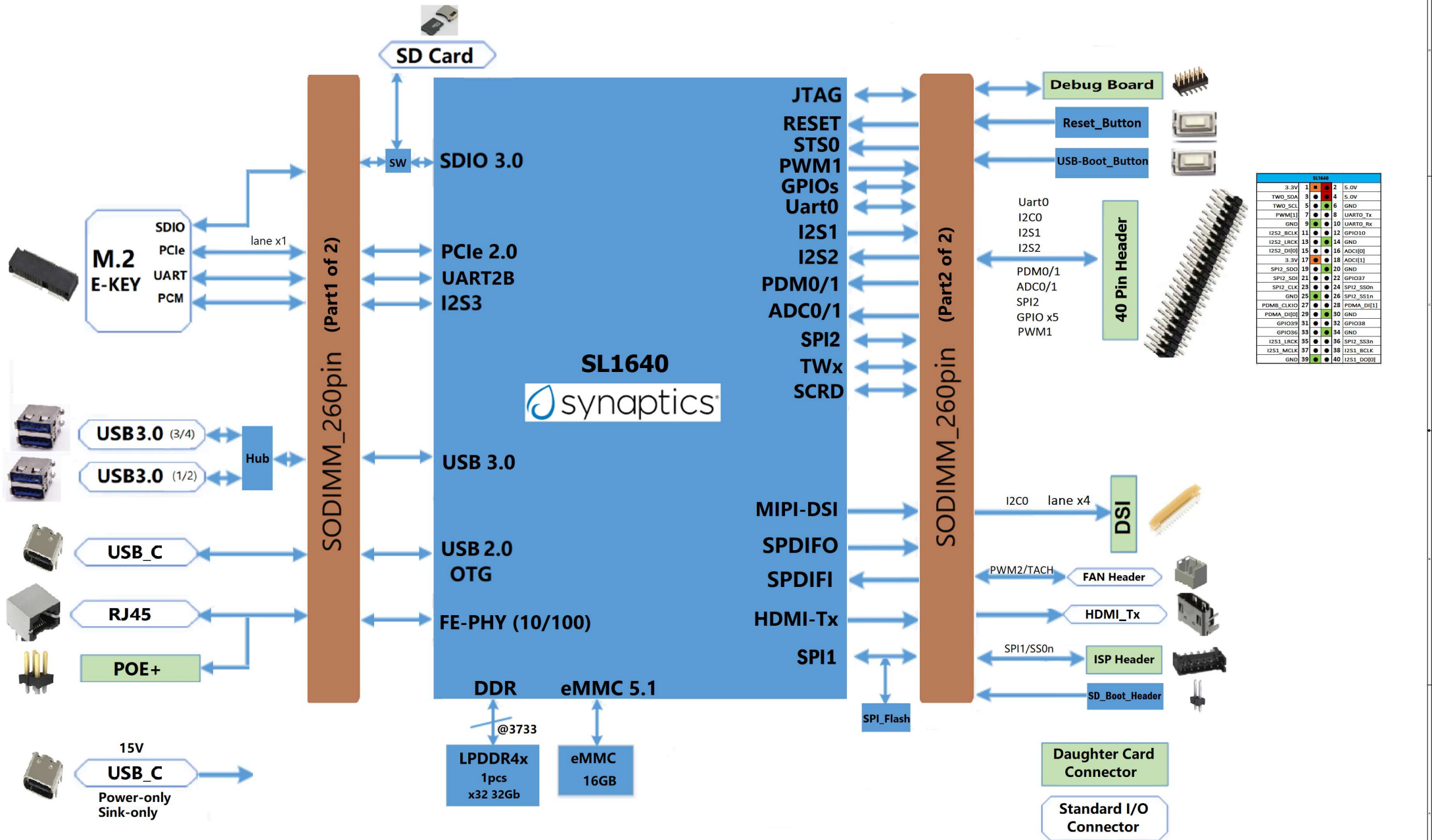
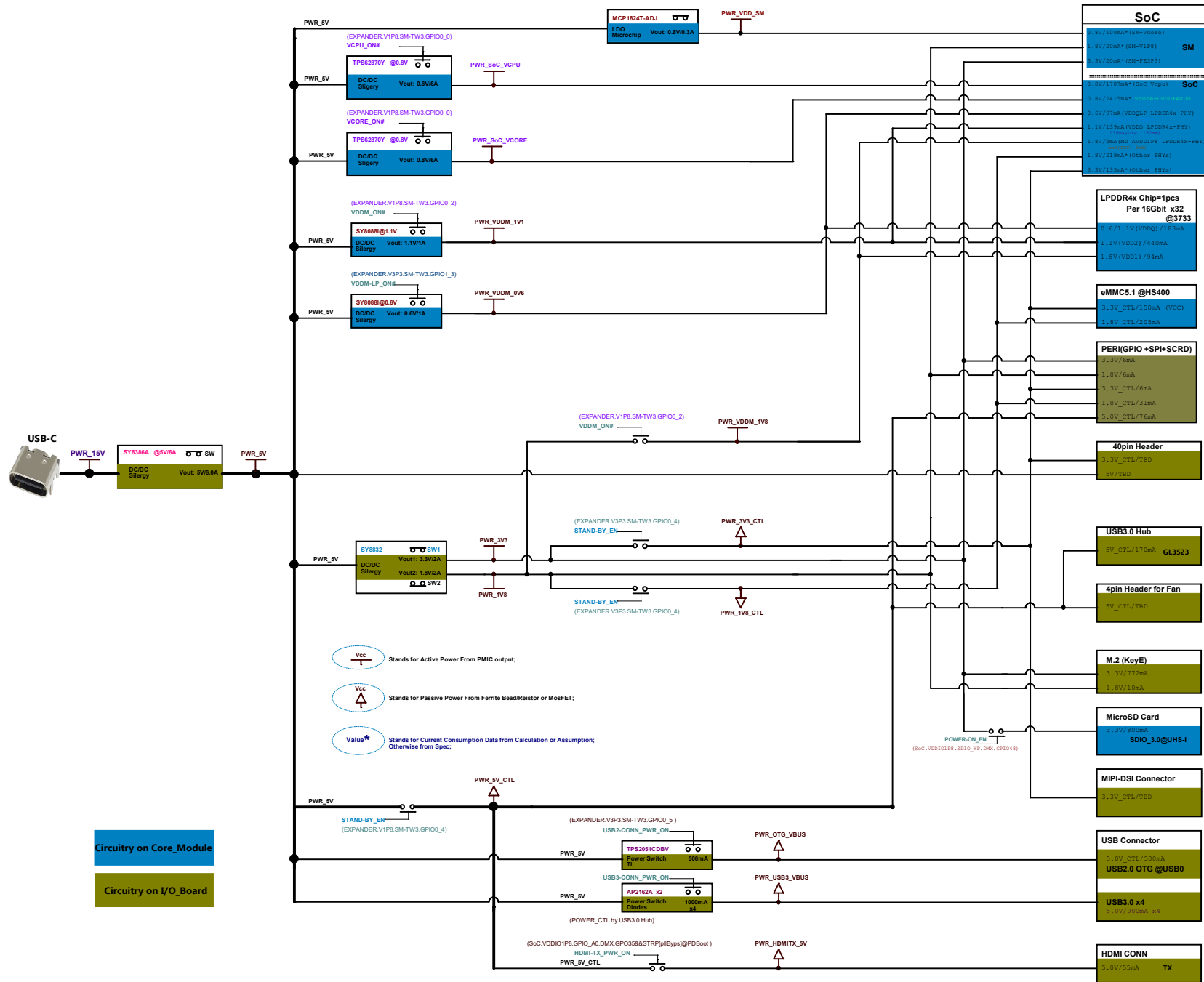


# SL1640 CORE MODULE Schematics

## Block Diagram



# Power Tree



REVISION HISTORY

Rev#	Date	Originator(s)	Rev Item ID	What Revised	Why Revised	SW Impacts	Other Impacts	Rework# Base On Previous Version	SW Strap [3:1]=b' '
A	11/13/2023	William W	1	Preliminary SCH for SL1640	SL1640-RDK design	NO	NO	NO	000
	11/22/2023	William W	2	Change 25Mhz crystal footprint from 3.2*2.5mm to 2.0*1.6mm	optimize PCB layout				
	12/11/2023		3	Change SD - Boot selection by jumper on I/O - Board	Clear for Boot - selection.				
B	01/19/2024	William W	1	Change R135=2.2K from DNS	Keep STRP[SM_SS0] is Low during AC/ON and RESET, avoid external Uart tool impact.	NO	NO	Rework A	000
C	04/11/2024	William W	1	Update Block Diagram with adding SD_Boot_Header.	Match with I/O-board changes	YES	NO	NO	100
			2	Change R1955, R1957 to 33R.	EMI improvement				
			3	Change R173 to 22R, mount on R1969, C1340					
			4	Add Page-21 for current sensors and do changes accordingly.	Monitor power rails				
			5	Change R120 to 2.2K from DNS.	Update SW Strap to 3b'100				
D	05/21/2024	William W	1	Update Synaptics Tittle Block	Update Synaptics Tittle Block	NO	NO	NO	100
			2	Change C1343=0.1uF, C1342=1K.	Optimize SD power sequence				
E	06/28/2024	William W	1	Update power test pads to 40mil from 18mil	Manufactuer requirement	NO	NO	NO	100
			2	Add 4 standoffs for mounting heatsink	Manufactuer requirement				
			3	Update LPDDR4x default size to 4GB	New requirement				
F	12/03/2024	William W	1	Correct the net alias on eMMC CMD and STRB pins	Correct net alias	NO	NO	NO	100

## SL1640 RDK I/O Reference

For details, please refer to  
SL1640\_RDK\_IO\_reference.xlsx;

\*\* Pinmux for Standard Interface sheet

\*\* Pinmux for GPIO sheet

\*\* GPIO Expander over I2C sheet

\*\* I2C Bus sheet

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**04: PIN-DeMUX TABLE**

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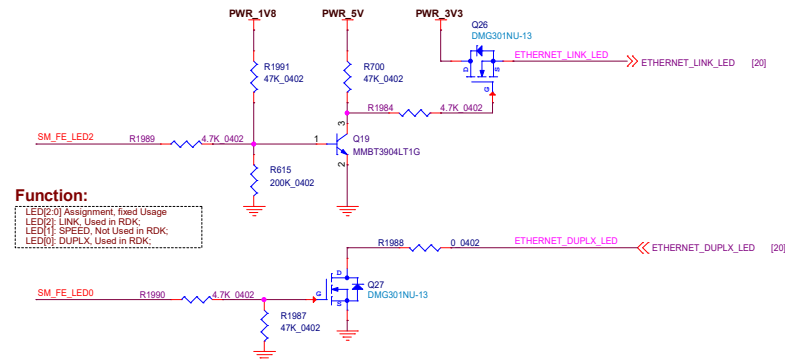
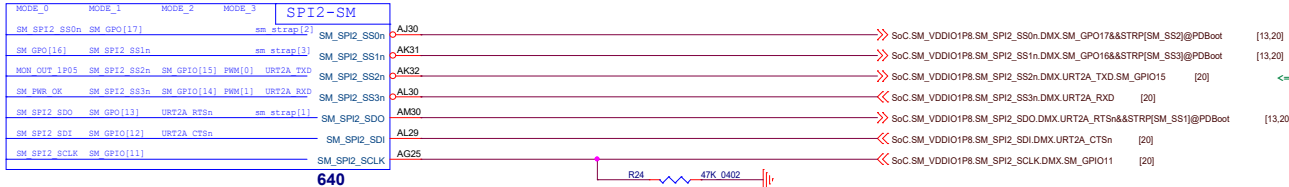
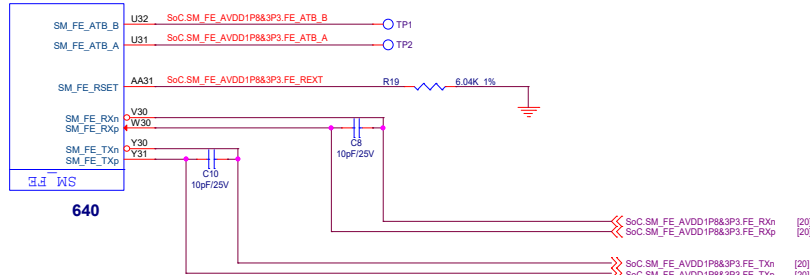
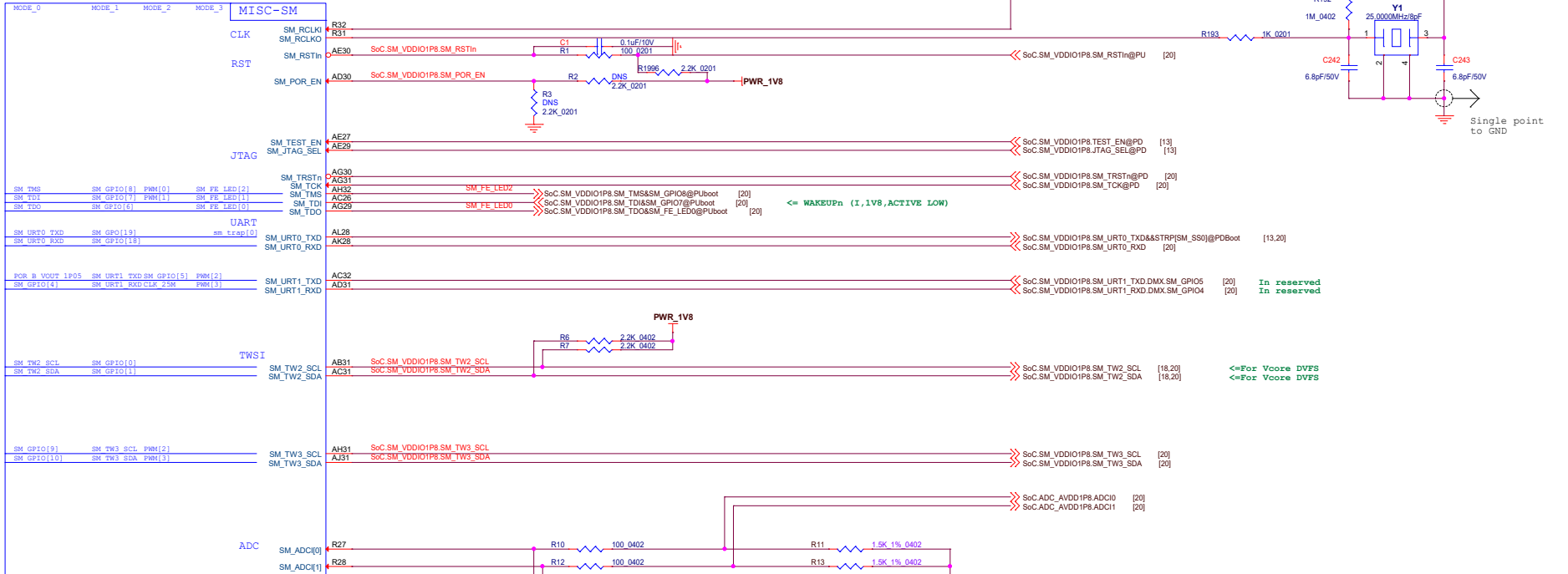
**SC950-000799-01**

Rev

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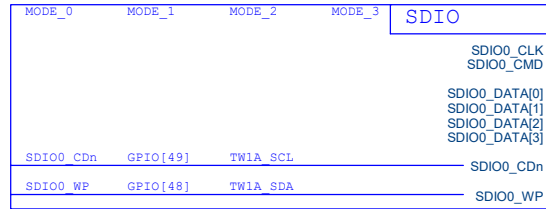
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Sheet 4 of 21



LED[2:0] Assignment, fixed Usage  
LED[2]: LINK, Used in RDK;  
LED[1]: SPEED, Not Used in RDK;  
LED[0]: DUPLX, Used in RDK;

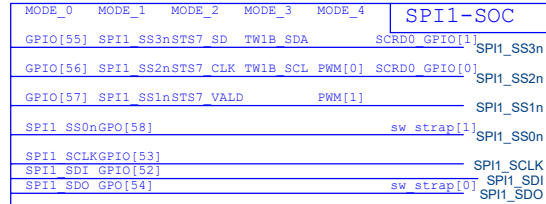
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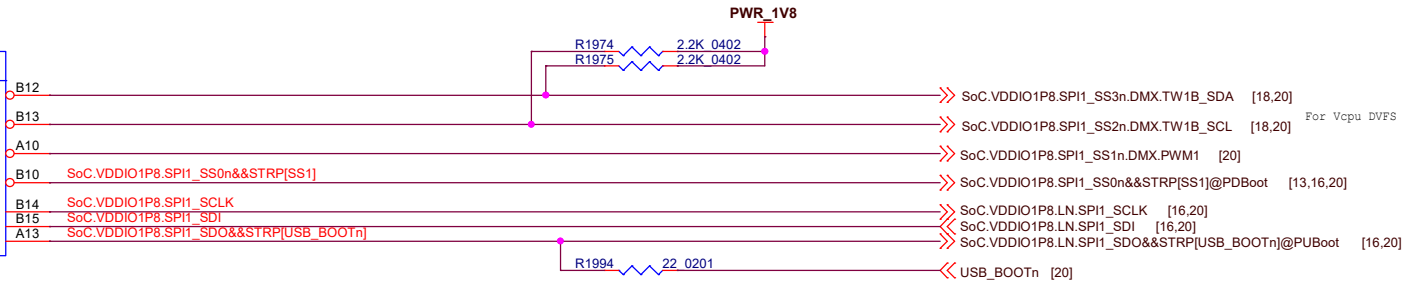
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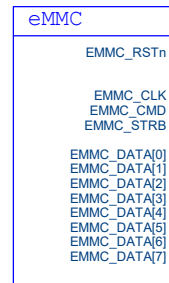
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## U1-6



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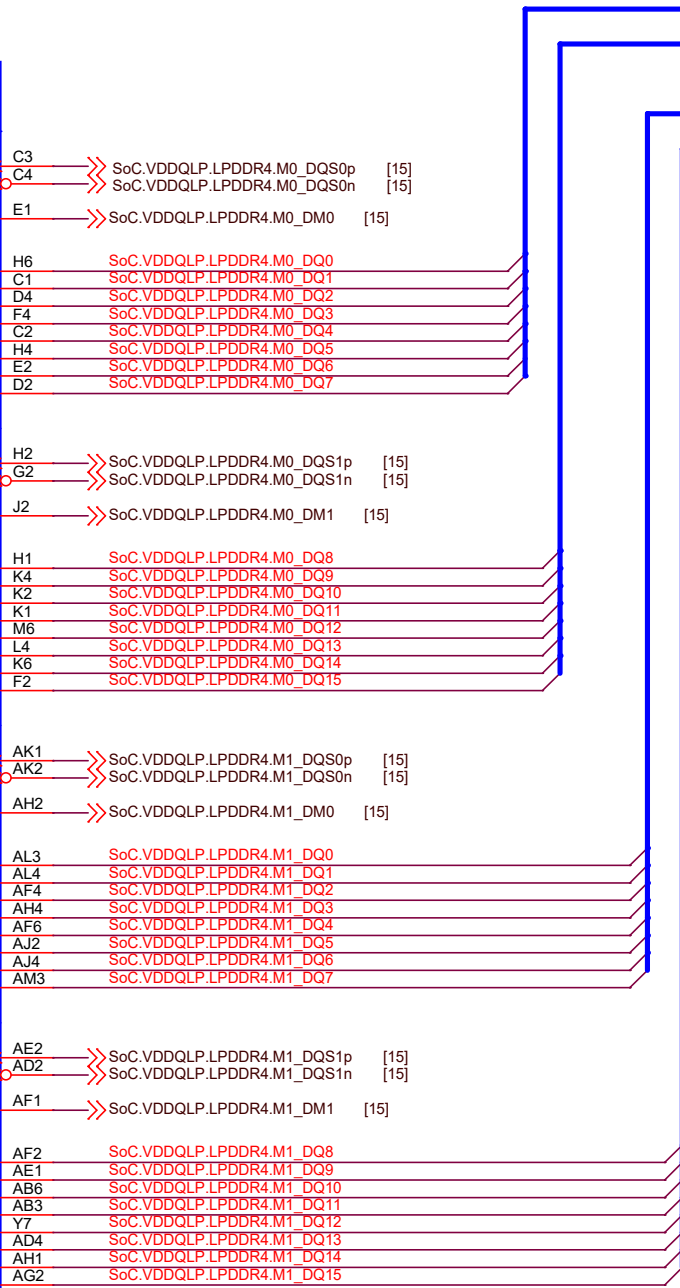
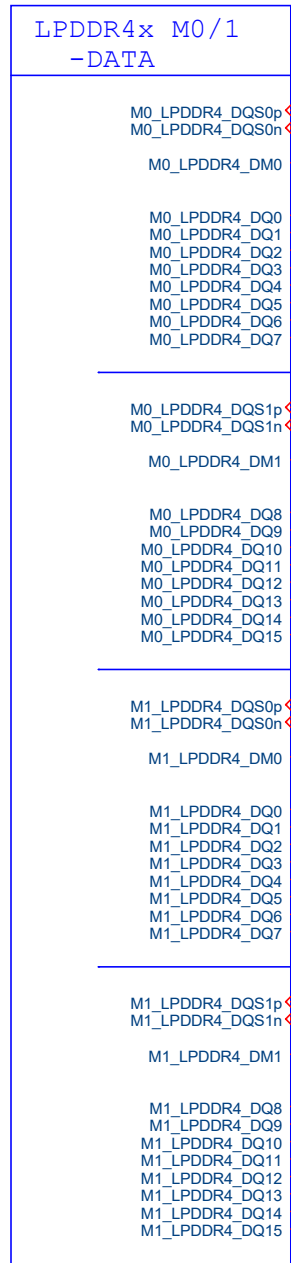


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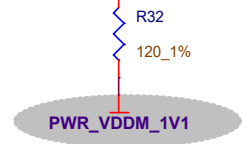
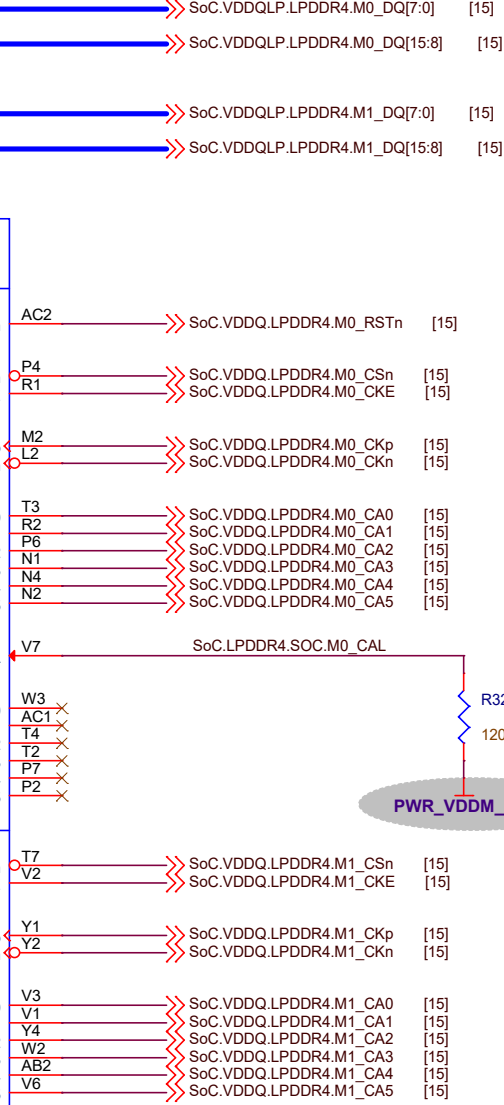
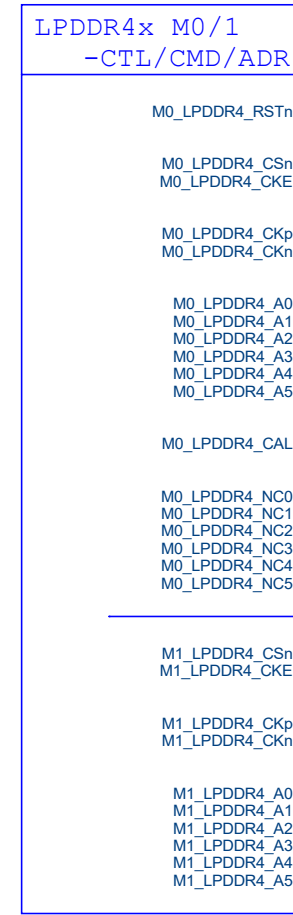
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Title <b>06: SDIO,SPI,eMMC</b>		
Size	Document Number <b>SC950-000799-01</b>	Rev <b>F</b>
Date	Wednesday, February 05, 2025	Sheet 6 of 21

# U1-3



# U1-2



640

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Title  
**07: LPDDR4x PHY**

Size  
Document Number  
**SC950-000799-01**

Date: Wednesday, February 05, 2025 Sheet 7 of 21

Rev  
F

## U1-9

MODE_0	MODE_1	MODE_2	MODE_3	MODE_4	I2S/SPDIF
GPIO[18]	I2S1_MCLK		STS2_SOP		I2S1_MCLK
GPIO[20]	I2S1_BCLKIOPWM[1]				I2S1_BCLK
GPIO[21]	I2S1_LRCKIOPWM[0]	ARC TEST OUT			I2S1_LRCK
GPO[19]	I2S1_DO[0]		legacy boot		I2S1_DO[0]
GPIO[17]	I2S1_DO[1]	STS2_CLK			I2S1_DO[1]
GPIO[16]	I2S1_DO[2]	PWM[2]	STS2_SD		I2S1_DO[2]
GPIO[15]	I2S1_DO[3]	PWM[3]	STS2_VALD		I2S1_DO[3]
GPIO[12]	I2S2_BCLKIOPDMA_CLKIO				I2S2_BCLK
GPIO[13]	I2S2_LRCKIO				I2S2_LRCK
GPIO[11]	I2S2_DI[0]				I2S2_DI[0]
GPIO[10]	I2S2_DI[1]		STS4_VALD		I2S2_DI[1]
GPIO[9]	I2S2_DI[2]	PDMA_DI[1]	STS4_CLK		I2S2_DI[2]
GPIO[8]	I2S2_DI[3]	PDMA_DI[0]	STS4_SD		I2S2_DI[3]
GPO[7]	I2S2_MCLK	PDMA_CLKIO	HDMI_FBCLK boot_src[0]		I2S2_MCLK
GPIO[3]	I2S3_LRCKIO		STS3_CLK		I2S3_LRCK
GPIO[2]	I2S3_BCLKIO		STS3_SD		I2S3_BCLK
GPIO[0]	I2S3_DI		STS3_VALD		I2S3_DI
GPIO[1]	I2S3_DO		STS3_SOP		I2S3_DO
GPIO[4]	SPDIFI	PDMA_DI			SPDIFI
GPO[14]	SPDIFO		AVPLL_CLKO boot_src[1]		SPDIFO

640

AL8	SoC.VDDIO1P8.I2S1_MCLK	>>>	SoC.VDDIO1P8.I2S1_MCLK.DMX.STS2_SOP	[20]	
AM10	SoC.VDDIO1P8.I2S1_BCLK	>>>	SoC.VDDIO1P8.LN.I2S1_BCLK	[20]	
AK11	SoC.VDDIO1P8.I2S1_LRCK	>>>	SoC.VDDIO1P8.LN.I2S1_LRCK	[20]	
AL13	SoC.VDDIO1P8.I2S1_DO0&&STRP[legacy_boot]	>>>	SoC.VDDIO1P8.LN.I2S1_DO0&&STRP[legacy_boot]@PDBoot	[13,20]	
AM13	SoC.VDDIO1P8.I2S1_DO1	>>>	SoC.VDDIO1P8.DMX.I2S1_DO1.GPIO17	[17]	<=SD_VOL-SEL (0,0=1V8, 1=3V3)
AL11	SoC.VDDIO1P8.I2S1_DO2	>>>	SoC.VDDIO1P8.DMX.I2S1_DO2.GPIO16.PWM[2]	[20]	<=PWM[2] for Fan
AK13	SoC.VDDIO1P8.I2S1_DO3	>>>	SoC.VDDIO1P8.DMX.I2S1_DO3.GPIO15.PWM3	[20]	<=USB-C-logic_INTn
AF13	SoC.VDDIO1P8.I2S2_BCLK	<<<	SoC.VDDIO1P8.DMX.I2S2_BCLK	[20]	
AG11	SoC.VDDIO1P8.I2S2_LRCK	<<<	SoC.VDDIO1P8.LN.I2S2_LRCK	[20]	
AJ9	SoC.VDDIO1P8.I2S2_DI0	<<<	SoC.VDDIO1P8.DMX.I2S2_DI0	[20]	
AK9	SoC.VDDIO1P8.DMX.I2S2_DI1.GPIO10	<<<	SoC.VDDIO1P8.DMX.I2S2_DI1.GPIO10	[20]	
AM8	SoC.VDDIO1P8.I2S2_DI2.DMX.PDMA_DI1	<<<	SoC.VDDIO1P8.I2S2_DI2.DMX.PDMA_DI1	[20]	
AG9	SoC.VDDIO1P8.I2S2_DI3.DMX.PDMA_DI0	<<<	SoC.VDDIO1P8.I2S2_DI3.DMX.PDMA_DI0	[20]	
AF9	SoC.VDDIO1P8.I2S2_MCLK&&STRP[boot_src0]	>>>	SoC.VDDIO1P8.I2S2_MCLK&&I2S2_BCLK.DMX.PDM_CLKO&&STRP[boot_src0]@PDBoot	[13,20]	
AL6	SoC.VDDIO1P8.I2S3_LRCK	<<<	SoC.VDDIO1P8.DMX.I2S3_LRCK	[20]	
AL5	SoC.VDDIO1P8.I2S3_BCLK	<<<	SoC.VDDIO1P8.DMX.I2S3_BCLK	[20]	
AG7	SoC.VDDIO1P8.I2S3_DI	<<<	SoC.VDDIO1P8.DMX.I2S3_DI	[20]	
AJ7	SoC.VDDIO1P8.I2S3_DO	<<<	SoC.VDDIO1P8.DMX.I2S3_DO	[20]	
AK10	SoC.VDDIO1P8.SPDIFI	>>>	SoC.VDDIO1P8.DMX.SPDIFI.GPIO4	[20]	<=GPIO4 for Fan_TACH
AL10	SoC.VDDIO1P8.SPDIFO&&STRP[boot_src1]	>>>	SoC.VDDIO1P8.LN.SPDIFO&&STRP[boot_src1]@PUBoot	[13,20]	In reserved

## U1-8

MODE_0	MODE_1	MODE_2	MODE_3	MODE_4	STS IN
GPIO[43]	STS0_CLK CPUPLL_CLKO		URT2B_RXD		STS0_CLK
GPIO[42]	STS0_SOP SYSPLL_CLKOSTS5_CLK		URT2B_TXD		STS0_SOP
GPIO[41]	STS0_SD MEMPLL_CLKO		URT2B_CTSn		STS0_SD
GPIO[40]	STS0_VALD	STS5_SD	URT2B_RTSn		STS0_VALD
GPIO[39]	STS1_CLK	PWM[0]			STS1_CLK
GPIO[38]	STS1_SOP	PWM[1]	STS6_CLK		STS1_SOP
GPIO[37]	STS1_SD	PWM[2]			STS1_SD
GPIO[36]	STS1_VALD	PWM[3]	STS6_SD		STS1_VALD

640

B5		<<<	SoC.VDDIO1P8.STS0_CLK.GPIO43.URT2B_RXD	[20]	
B6		<<<	SoC.VDDIO1P8.STS0_SYNC.GPIO42.URT2B_TXD	[20]	
B7		<<<	SoC.VDDIO1P8.STS0_DAT.GPIO41.URT2B_CTSn	[20]	
A6		<<<	SoC.VDDIO1P8.STS0_VALD.GPIO40.URT2B_RTSn	[20]	
B8		>>>	SoC.VDDIO1P8.STS1_CLK.GPIO39	[20]	
A8		>>>	SoC.VDDIO1P8.STS1_SYNC.GPIO38	[20]	
C10		>>>	SoC.VDDIO1P8.STS1_DAT.GPIO37	[20]	
C11		>>>	SoC.VDDIO1P8.STS1_VALD.GPIO36	[20]	

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08: I2S/SPDIF,STS

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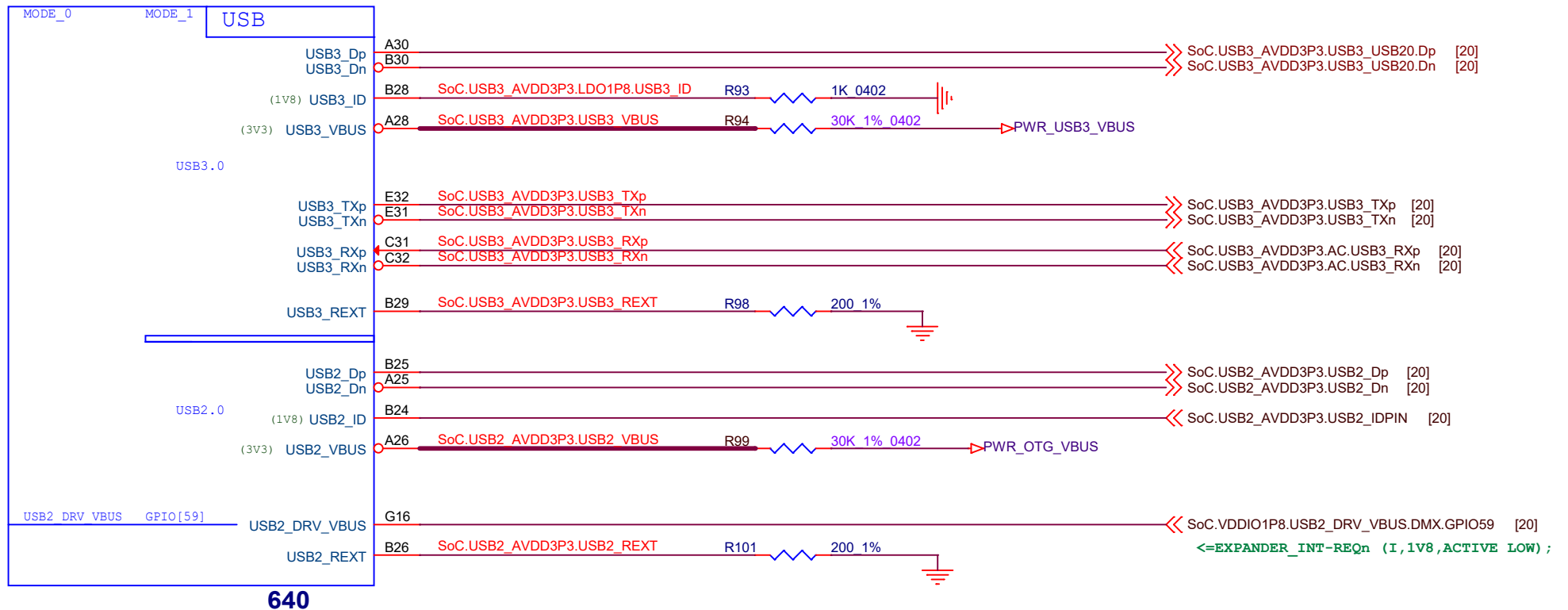
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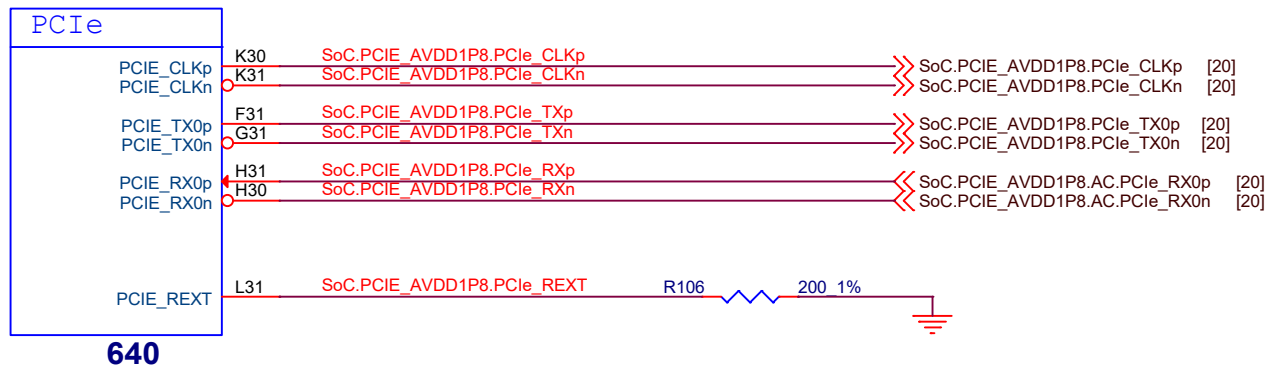
8 of 21



# U1-14



# U1-13



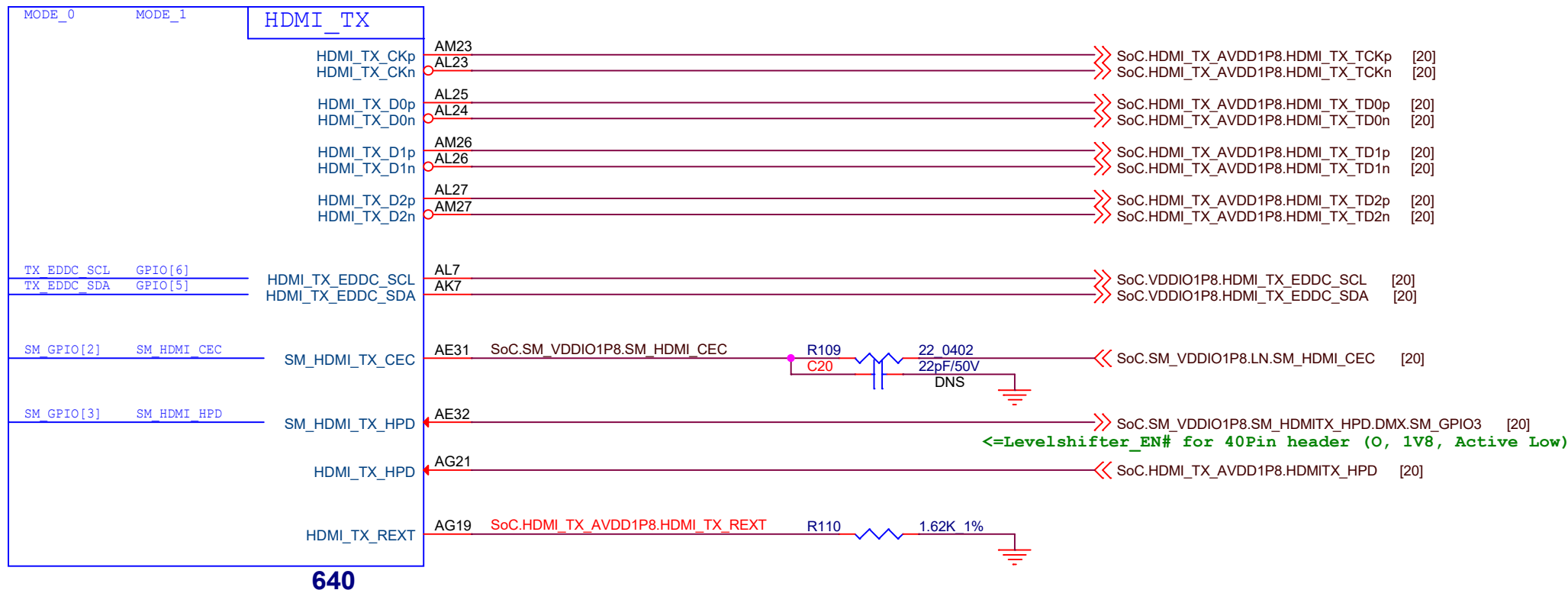
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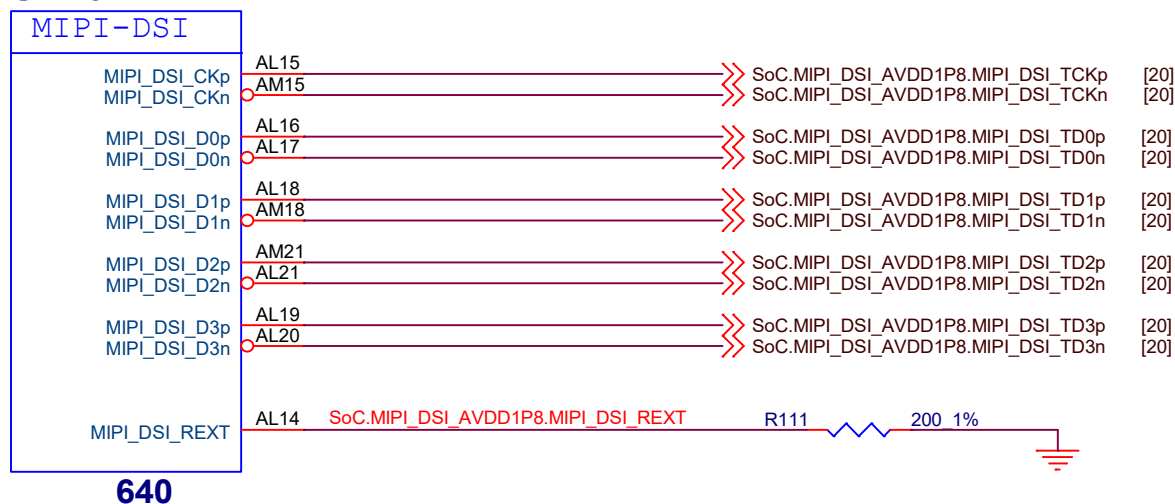


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Size	Document Number	Rev
	<b>SC950-000799-01</b>	<b>F</b>
Date:	Wednesday, February 05, 2025	Sheet 9 of 21

# U1-11



# U1-15



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**Title**  
**10: HDMI\_Tx,MIPI\_DSI**

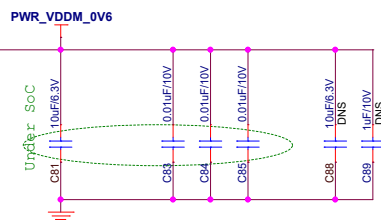
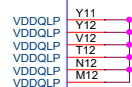
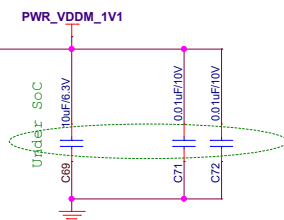
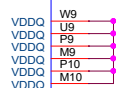
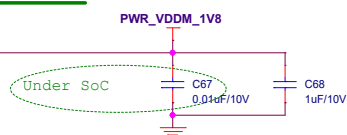
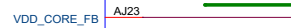
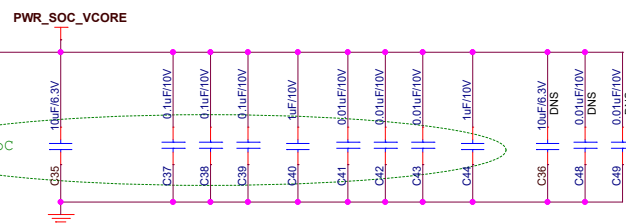
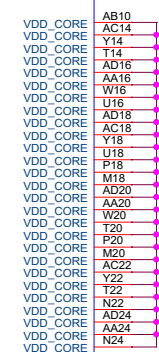
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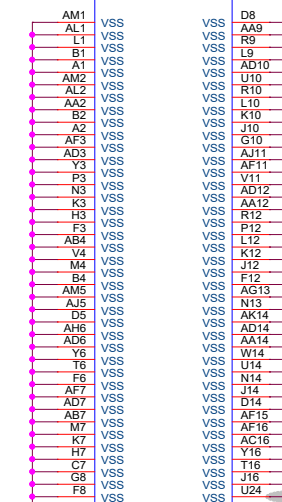
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**Sheet** 10 **of** 21



## POWER-SOC VDD/VDDM



## GND

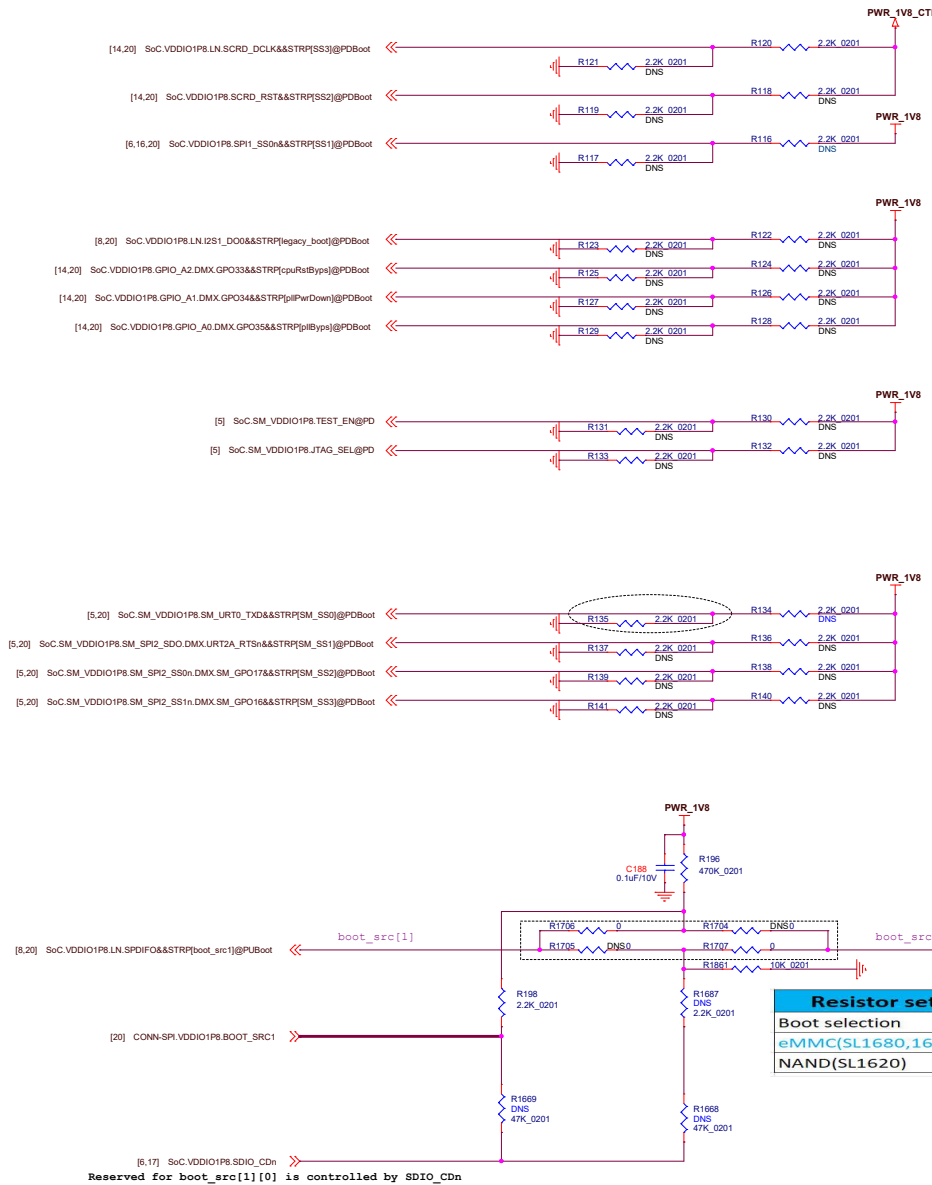


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## SL1640 LP4x DDR Parameters & Configuration Table

SETTING	SM_STRP[3:1]	VENDOR	P/N#	DENSITY	QTY.	SPEED	RTT	VTT-REG.	LAYER Count
0	3b'000'	Micron	MT53E512M32D2NF-053	16GbIt x32	x1	@3733	No,ODT	No,ODT	4L

S.No	Pad Name	Strap name	Description	on-chip PU/PD
1	SPDIFO	boot_src[1]	CPU Boot Source bit[1]	PU
2	I2S2_MCLK	boot_src[0]	CPU boot source bit[0]: 00: ROM boot from SPI 01: Reserved 10: ROM boot from EMMC 11: Direct boot from SPI(Only available when ENG_EN=1) When direct boot from SPI(SPI clear boot), pwrCntlByps and cpuRstByps should be set to 1, pllByps Strap should be set to 0, pllPwrDown should be set to 0	PD
3	SPI1_SDO	software_strap[0](USB_BOOTn)	Straps for software usage ROM code will use this strap to decide booting from USB or not 0: Boot from USB 1: Boot from the device select by boot_src	PU
4	SPI1_SS0n	software_strap[1]	Straps for software usage	PD
5	I2S1_DQ[0]	legacy_boot	Strap to reduce reset wait time 0: 2ms 1: 20ms	PD
6	SCRD0_RST	software_strap[2]	Straps for software usage	PD
7	SCRD0_DCLK	software_strap[3]	Straps for software usage	PD
8	GPIO_A[2]	cpuRstByps	CPU reset bypass strap 0: Enable reset logic inside cpu partition 1: Bypass reset logic inside cpu partition	PD
9	GPIO_A[1]	pllPwrDown	SYS/MEM/CPU PLL Power Down 1: Power Down 0: Power UP	PD
10	GPIO_A[0]	pllByps	SYS/MEM/CPU PLL Bypass indicator 0: No Bypass 1: All PLL Bypassed	PD
11	SM_URT0_TXD	SM_STRP[0]	SM to SOC RStn mode select 0: socRstN releasing waits for SoCrstCnt but does not wait for SM_PWR_OK(mode_0 of SM_URT0_TXD, system will assert this signal when SOC core power is ready). 1: socRstN releasing waits for both SoCrstCnt and SM_PWR_OK.	PD
12	SM_SPI2_SDO	SM_STRP[1]	software strap	PD
13	SM_SPI2_SS0n	SM_STRP[2]	software strap	PD
14	SM_SPI2_SS1n	SM_STRP[3]	software strap	PD



Resistor settings for SL1680,SL1640,SL1620				
Boot selection	R1706	R1705	R1704	R1707
eMMC(SL1680,1640,1620)	OR	DNS	DNS	OR
NAND(SL1620)	DNS	OR	OR	DNS

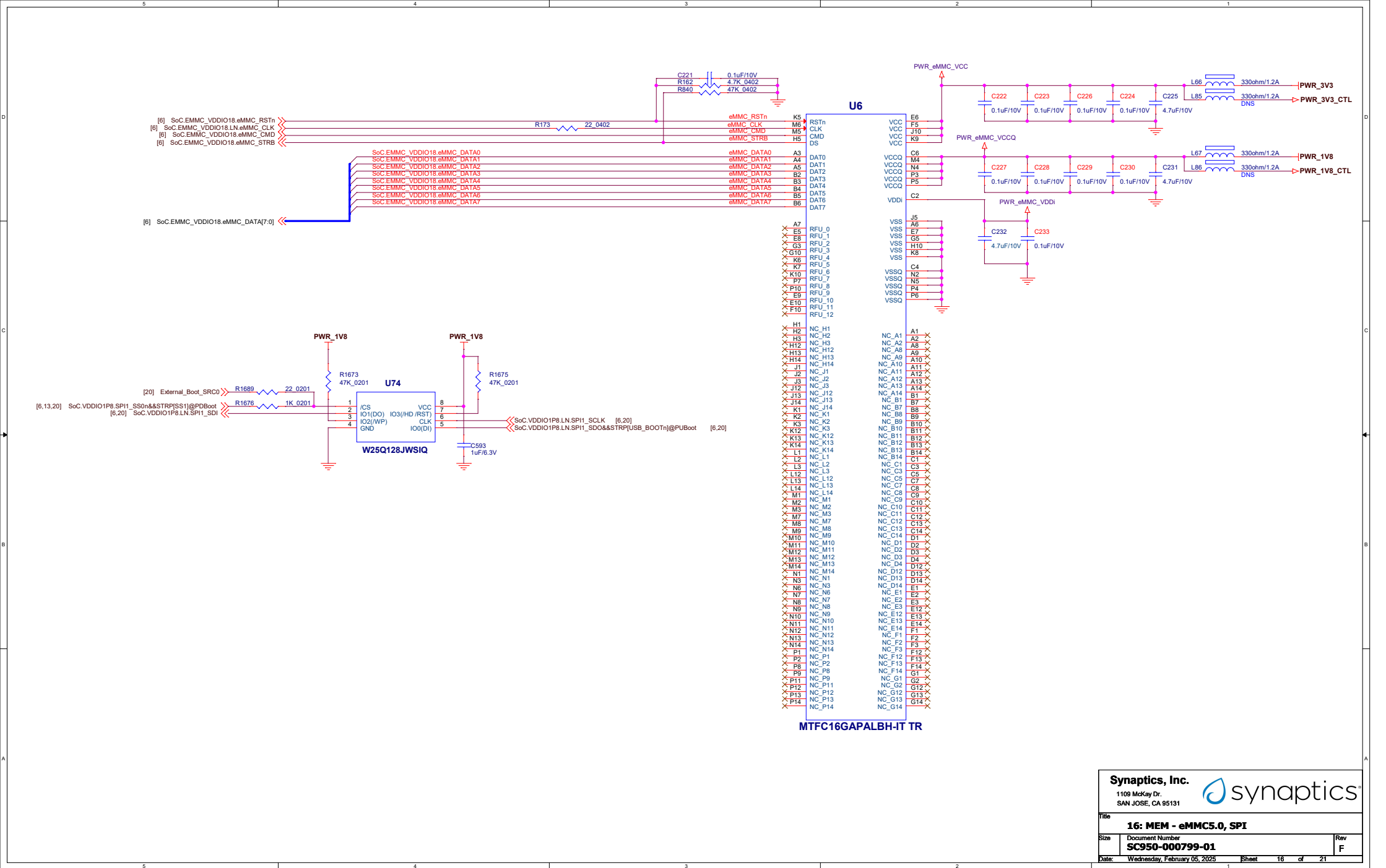
MODE_0	MODE_1	MISC-SOC
GPO[35]	STRP pllByps	GPIO_A[0]
GPO[34]	pllPwrDown	GPIO_A[1]
GPO[33]	cpuRstByps	GPIO_A[2]
		TWSI
GPIO[51]	TW0_SCL	TW0_SCL
GPIO[50]	TW0_SDA	TW0_SDA

Pin	Signal	Function	Notes
G12	SoC.VDDIO1P8.GPIO_A0.DMX.GPO35&&STRP[pllByps]@PDBoot	[13,20]	
F10	SoC.VDDIO1P8.GPIO_A1.DMX.GPO34&&STRP[ppllPwrDown]@PDBoot	[13,20]	
D6	SoC.VDDIO1P8.GPIO_A2.DMX.GPO33&&STRP[cpuRstByps]@PDBoot	[13,20]	
G14	SoC.VDDIO1P8.TW0_SCL	[20]	
F14	SoC.VDDIO1P8.TW0_SDA	[20]	

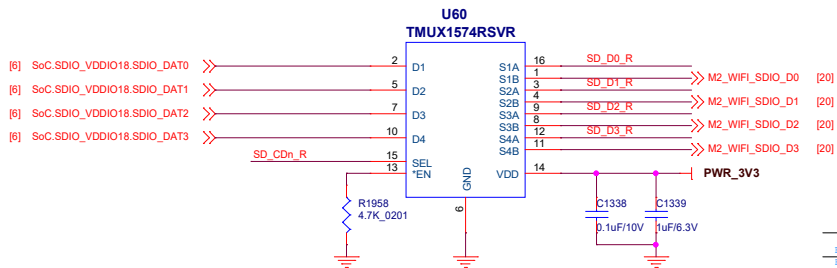
MODE_0	MODE_1	SCRD
SCRD0_RST	GPO[47] sw strap[2]	SCRD0_RST
SCRD0_DCLK	GPO[46] sw strap[3]	SCRD0_DCLK
SCRD0_DIO	GPIO[45]	SCRD0_DIO
SCRD0_CRD PRES	GPIO[44]	SCRD0_CRD_PRES

M31	SoC.VDDIO1P8.SCRD_RST&&STRP[SS2]	SoC.VDDIO1P8.SCRD_RST&&STRP[SS2]@PDBoot [13,20]	In reserved
M32	SoC.VDDIO1P8.SCRD_DCLK&&STRP[SS3]	SoC.VDDIO1P8.LN.SCRD_DCLK&&STRP[SS3]@PDBoot [13,20]	In reserved
P31	SoC.VDDIO1P8.SCRD_DIO	SoC.VDDIO1P8.LN.SCRD_DIO [20]	In reserved
N31	SoC.VDDIO1P8.SCRD_PRES	SoC.VDDIO1P8.SCRD_PRES [20]	In reserved

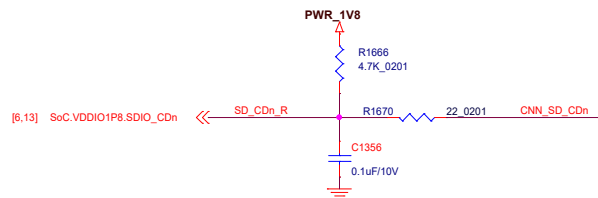
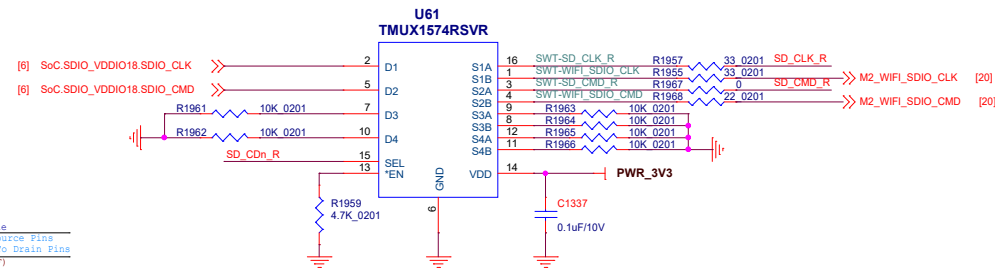




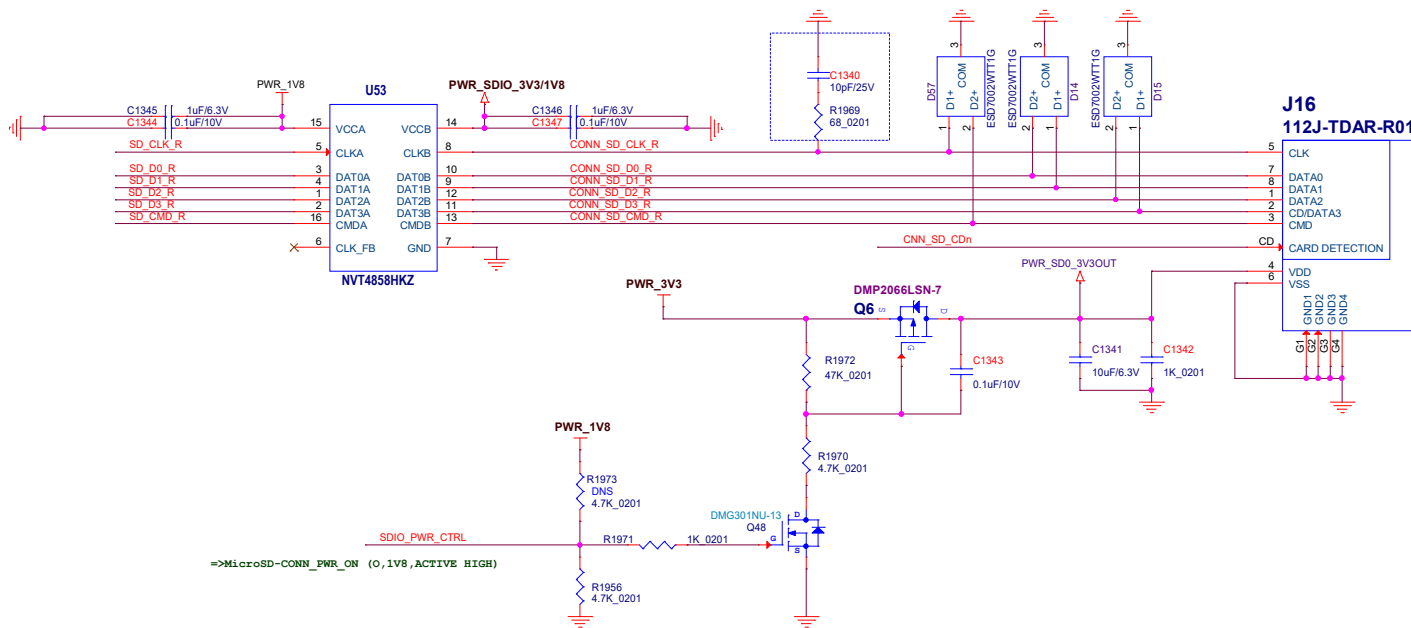




Function Table		
Selected Source Pins		
EN	SEL	Connected To Drain Pins
L	X	HI-Z (OFF)
L	L	S1A connected to D1 S2A connected to D2 S3A connected to D3 S4A connected to D4
L	H	S1B connected to D1 S2B connected to D2 S3B connected to D3 S4B connected to D4



PWR_LS_SD	GPIO_CTRL	Bus Speed mode
1.8V	LOW	UHS
3.3V	HIGH	DS/HS (DEFAULT)



## Default 0.8V/6A for SOC VDD\_CORE;

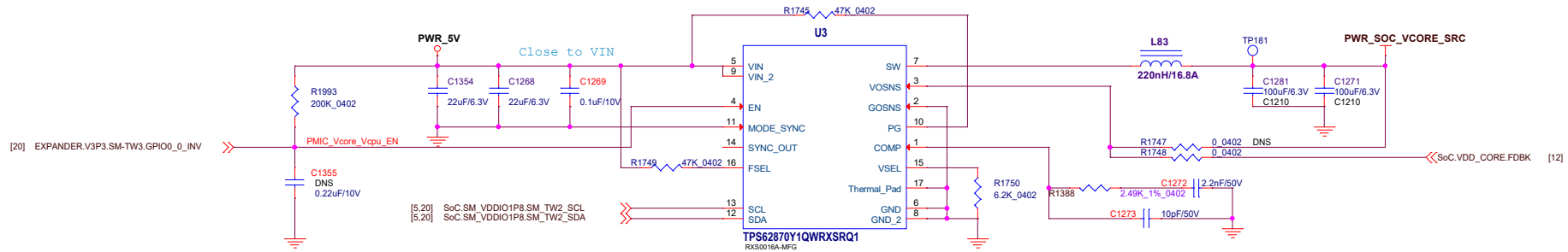


Table For 6A and 9A PMIC

Current	P/N#	Freq	Slave Add(7-bit)	Cout	L
6A	TPS62870Y1QWRXSRQ1	2.5MHz	0x40	100uF x2	220nH (XAL4020-221MEC)
9A	TPS62871Y1QWRXSRQ1	2.5MHz	0x40	100uF x2	100nH (IHLP2020CZERR10M11)

6A: R1388=2.49K

9A: R1388=1.78K

## Default 0.8V/6A for SOC VDD\_CPU;

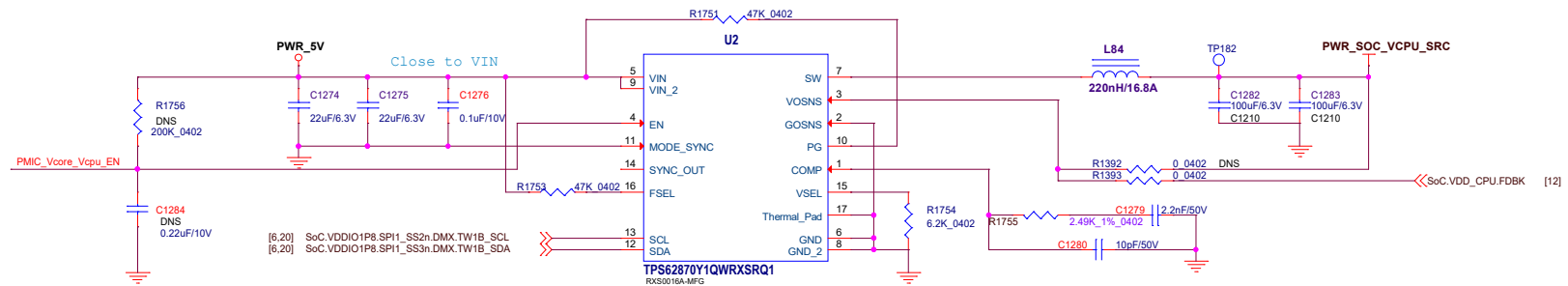


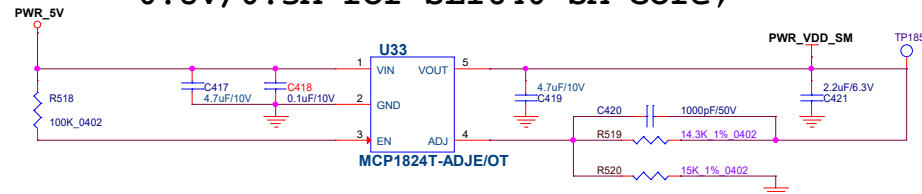
Table For 6A and 9A PMIC

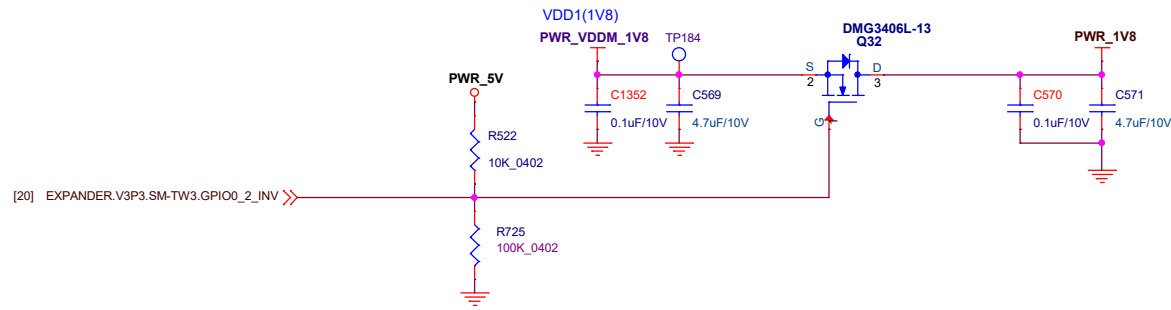
Current	P/N#	Freq	Slave Add(7-bit)	Cout	L
6A	TPS62870Y1QWRXSRQ1	2.5MHz	0x40	100uF x2	220nH (XAL4020-221MEC)
9A	TPS62871Y1QWRXSRQ1	2.5MHz	0x40	100uF x2	100nH (IHLP2020CZERR10M11)

6A: R1755=2.49K

9A: R1755=1.78K

## 0.8V/0.3A for SL1640 SM-Core;



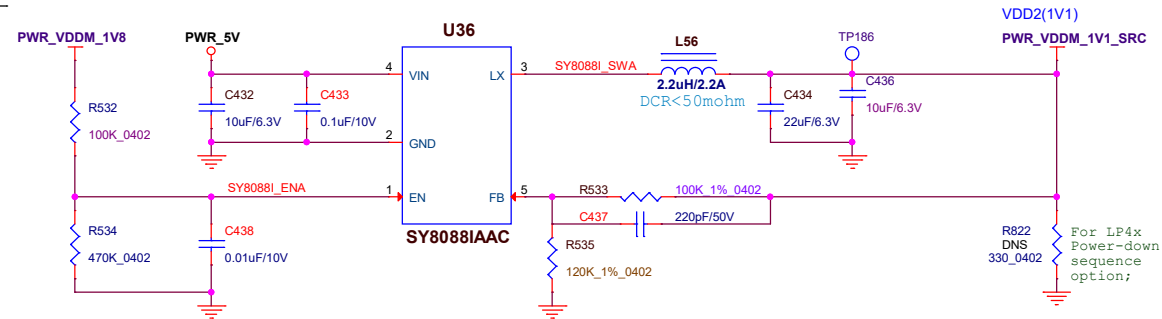
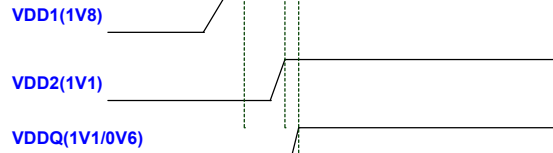


## 1.1V/1A for DDR-SOC + DDR-DEVICE;

### LPDDR4x Power supply voltage ramp requirements:

- 1)VDD1 must ramp at the same time or earlier than VDD2.
- 2)VDD2 must ramp at the same time or earlier than VDDQ.  
i.e., VDD1>=VDD2>=VDDQ on power-up sequence.

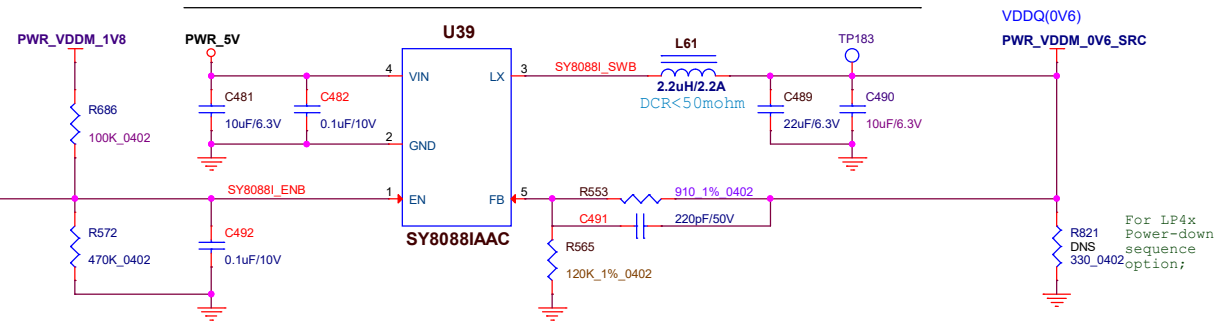
### Power-Up Sequence For LPDDR4x DEVICE



## 0.6V/1A for DDR-SOC + DDR-DEVICE;

### Power for proper Self Refresh operation:

- 1)Power supply pins (VDD1, VDD2 and VDDQ) must be at valid levels.
- 2)VDDQ may be turned off during Self-Refresh with Power Down after tCKELCK (Max(5ns,5nCK)) is satisfied (Refresh to figure about tCKELCK). Prior to exiting Self-Refresh with Power Down, VDDQ must be within specified limits.



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Title		
19: PWR-VDDM_1V8/1V1/0V6		
Size	Document Number	Rev
	SC950-000799-01	F
Date:	Wednesday, February 05, 2025	Sheet 19 of 21

